NONVOLATILE MEMORY STRUCTURES AND FABRICATION METHODS

Chung Wai Leung
Chia-Shun Hsiao
Vei-Han Chan

ABSTRACT OF THE DISCLOSURE

To fabricate a semiconductor memory, one or more pairs of first structures are formed over a semiconductor substrate. Each first structure comprises (a) a plurality of floating gates of memory cells and (b) a first conductive line providing control gates for the memory cells. The control gates overlie the floating gates. Each pair of the first structures corresponds to a plurality of doped regions each of which provides a source/drain region to a memory cell having the floating and control gates in one or the structure and a source/drain region to a memory cell having floating and control gates in the other one of the structures. For each pair, a second conductive line is formed whose bottom surface extends between the two structures and physically contacts the corresponding first doped regions. In some embodiments, the first doped regions are separated by insulation trenches. The second conductive line may form a conductive plug at least partially filling the region between the two first structures.